

WHAT IS CLAIMED IS:

1. A buffered memory module test fixture comprising:

a circuit board having

a first electrical connector to receive a first buffered memory module under test,

5 a master memory buffer connection point, and

a first set of electrical traces, corresponding to a first point-to-point memory channel,
connecting the electrical connector with the master memory buffer connection point; and

a control bus routed to the master memory buffer connection point, to propagate control
signals to a master memory buffer to cause the master memory buffer to exercise the memory
10 channel.

2. The buffered memory module test fixture of claim 1, further comprising the master
memory buffer.

15 3. The buffered memory module test fixture of claim 2, wherein the master memory buffer
has a host-side memory port, and wherein the host-side memory port is disconnected.

4. The buffered memory module test fixture of claim 2, wherein the master memory buffer
is mounted to the circuit board.

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5. The buffered memory module test fixture of claim 2, wherein the master memory buffer
connection point is a memory module electrical connector, and wherein the master memory
buffer is mounted on a master memory module card inserted into the memory module
electrical connector.

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6. The buffered memory module test fixture of claim 5, wherein the master memory module card further comprises a plurality of memory devices connected to the master memory buffer by a memory device channel.
- 5 7. The buffered memory module test fixture of claim 1, wherein the control bus is a system management bus.
8. The buffered memory module test fixture of claim 7, wherein the circuit board is configured for edge insertion in a computer peripheral bus slot, with the system management
10 bus routed to the insertion edge of the card for connection to a computer system management bus.
9. The buffered memory module test fixture of claim 1, further comprising at least one voltage regulator to supply operating power to a memory module and a master memory
15 buffer during test, and a clock generator to supply a reference clock signal to the memory module and the master memory buffer during test.
10. The buffered memory module test fixture of claim 1, further comprising the buffered memory module under test, comprising:
- 20 a module circuit board having a set of memory device channel traces with a take-off point for monitoring signals on at least selected memory device channel traces;
- a memory buffer connected to one end of the memory device channel traces;
- a memory module connector connected to the other end of the memory device channel traces; and
- 25 a memory module inserted in the memory module connector.

11. The buffered memory module test fixture of claim 10, further comprising additional circuitry or equipment connected to the take-off point to store or analyze memory channel behavior.

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12. The buffered memory module test fixture of claim 10, further comprising a proprietary or standard connection to additional circuitry or equipment.

13. The buffered memory module test fixture of claim 1, further comprising:

10 a second electrical connector to receive a second buffered memory module under test; and
 a second set of electrical traces, corresponding to a second point-to-point memory channel, connecting the second electrical connector with the first electrical connector.

14. The buffered memory module test fixture of claim 13, wherein the control bus is further
15 routed to the first electrical connector, to propagate control signals to a first buffered memory module, inserted in the first electrical connector, to cause that memory module to exercise the second memory channel independent of the first memory channel.

15. A memory module buffer comprising:

20 a host-side memory channel port, a downstream memory channel port, a control bus port, and a memory device port;

 transfer circuitry to relay memory channel data between the memory channel ports;

 memory access circuitry to reformat and relay data between the host-side memory channel port and the memory device port; and

25 control circuitry to cause the memory module buffer to send and receive memory channel

data over the downstream memory channel port in response to test commands received at the control bus port.

16. The memory module buffer of claim 15, the control circuitry further having the capability
5 to cause the memory module buffer to send and receive data over the memory device port in response to test commands received at the control bus port.

17. The memory module buffer of claim 15, wherein the control circuitry further comprises report circuitry to transmit test results from the control bus port.

10 18. A buffered memory module comprising:

a plurality of memory devices;

a host-side memory channel port, a downstream memory channel port, a control bus port,
and a memory device channel connected to the memory devices;

15 transfer circuitry to relay memory channel data between the host-side and downstream memory channel ports;

memory access circuitry to reformat and relay data between the host-side memory channel port and the memory device channel; and

control circuitry to send and receive memory channel data over the downstream memory
20 channel port in response to test commands received at the control bus port.

19. The buffered memory module of claim 18, the control circuitry further having the capability to cause data transfers with the memory devices in response to test commands received at the control bus port.

20. The buffered memory module of claim 18, wherein the control circuitry further comprises report circuitry to transmit test results from the control bus port.

21. A method of testing a memory channel independent of a host memory channel, the
5 method comprising:

connecting first and second memory module buffers to opposite ends of the memory channel;

issuing a control command to the first memory module buffer over a relatively low-speed bus independent of the host memory channel; and

10 in response to issuance of the control command, the first memory module buffer initiating a memory transaction over the memory channel to the second memory module buffer.

22. The method of claim 21, further comprising:

the second memory module buffer performing the initiated memory transaction; and

15 the first buffer reporting a result of the memory transaction over the low-speed bus.

23. The method of claim 21, wherein the memory channel comprises multiple point-to-point memory segments, each terminated by a memory module buffer at each end, the method further comprising the memory module buffers intermediate the first and second memory
20 module buffers relaying the memory transaction between the first and second memory module buffers.

24. The method of claim 21, further comprising locating the second memory module buffer on a module card with a connector for a memory module, using a memory module inserted in
25 the connector as memory for the module card, and monitoring signals passing to the memory

module during the memory transaction.

25. The method of claim 21, wherein the first and second buffers are respectively located on first and second memory modules inserted as system memory in a computer, the method
5 comprising the computer initiating the control command to test the memory channel independent of a host memory channel.

26. The method of claim 21, wherein connecting first and second memory module buffers to opposite ends of the memory channel comprises mounting the first memory module buffer on
10 a test fixture, connecting the first memory module buffer via a set of memory channel traces to a memory module connector on the test fixture, and inserting a memory module containing the second memory module buffer in the connector.

27. The method of claim 21, further comprising the first memory module buffer collecting
15 data from the low-speed channel, and then bursting that data to the second memory module buffer at memory channel operating speed.

28. An article of manufacture comprising computer-readable media containing instructions that, when executed by a processor, cause that processor to perform a method comprising:
20 transmitting commands over a system management bus to a first buffered memory module to cause that buffered memory module to exercise a memory channel between the first buffered memory module and a second buffered memory module; and
receiving results of the transmitted commands from the first buffered memory module over the system management bus.

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29. The article of manufacture of claim 28, wherein transmitting commands comprises at least one of reading and writing data to memory located on the second buffered memory module.

5 30. The article of manufacture of claim 28, the method further comprising selecting one of a plurality of buffered memory modules connected to the system management bus as the first buffered memory module, and addressing the transmitted commands to the selected memory module.

10 31. A computing device comprising:

a host memory controller;

at least first and second buffered memory modules;

a first point-to-point memory channel connecting the host memory controller to the first buffered memory module;

15 a second point-to-point memory channel connecting the first buffered memory module to the second buffered memory module;

a relatively low-speed bus coupled to the first buffered memory module; and

test circuitry on the first buffered memory module to receive commands over the low-speed bus and respond by issuing memory commands over the second point-to-point memory

20 channel to the second buffered memory module.

32. The computing device of claim 31, further comprising:

a third buffered memory module;

a third point-to-point memory channel connecting the second buffered memory module to

25 the third buffered memory module; and

test circuitry on the second buffered memory module to receive commands over the low-speed bus and respond by issuing memory commands over the third point-to-point memory channel to the third buffered memory module.

5 33. A memory module comprising:

 a plurality of memory devices;

 a host-side communications link port and a downstream communications link port;

 transfer circuitry to relay memory channel data between the host-side communications link port and the memory devices; and

10 self-test circuitry to facilitate one or more self tests selected from the group of tests consisting of a host-side communications link test between the memory module and a second device coupled to the host-side communications port, a downstream communication link test between the memory module and a second memory module, and a test of the plurality of memory devices.

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34. The memory module of claim 33, further comprising a control bus port, the memory module having the capability to control the self-test circuitry from the control bus port.